**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M.Tech I - Semester Examinations, April/May-2012**
**DIGITAL SYSTEM DESIGN**
(Common To DIGITAL SYSTEMS & COMPUTER ELECTRONICS, ELECTRONICS &
COMMUNICATION ENGINEERING, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI
DESIGN, SYSTEMS & SIGNAL PROCESSING, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM
DESIGN, DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS)

Time: 3hours                                                        Max. Marks: 60

**Answer any five questions**
**All questions carry equal marks**
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1.a)  Implement a bcd- to excess three code converter by ROM. Calculate the cross point
      density of the implementation.
  b)  For a pla with the following function
      $z1(x1x2x3) = x1$:    $z2(x1x2x3) = x1x2'+x1'x2$:   $z3(x1x2x3) = x2'x3+x2x3'$
      show the schematic diagram, show its ssr notation and draw nmos nor-nor
      implementation.

2.a)  Explain the Boolean difference method with an example.
  b)  A two level AND-OR circuit has four AND gates feeding one OR gate.
      The four AND gates realize the product terms x1x3'x4, x2x4, x1'x3'x4' and x1x2x3
      respectively. Derive the a and b - tests for detecting multiple stuck at faults.

3.a)  Explain podem with an example.
  b)  Explain transition count testing with an example.

4.    Find the minimized PLA of the following output Boolean function by a PLA minimizer.
      f1 = (2,4,5,6,7,10,14,15): f2 = (4,5,7,11,15)

5.a)  Draw the portion of an ASM chart that specify a conditional operation to increment
      register (r) during state t1 and transfer to state t2 if control inputs z and y are
      equal to 1 and 0 respectively.
  b)  Design an ASM chart for a serial adder with accumulator and show the control
      block diagram.

6.    Explain the procedure of designing a fault detection experiment with the help of an
      example.

7.    Construct a fault-detection experiment for the machine of the following table. That is
      entirely preset, that is with no initial adaptation part.

| Ps | Ns, z | |
|---|---|---|
| | X = 0, | x = 1 |
| A | D,0 | c,0 |
| B | C,0 | d,0 |
| C | A,0 | b,0 |
| D | D,1 | a,1 |

8.    Write short notes on the following.
  a)  Capabilities and limitations of FSM
  b)  Transition check approach in sequential circuits.
  c)  Bridging fault model.

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